REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-39 are pending in the application. The Examiner additionally stated that claims 1-39 are rejected. By this amendment, claims 2 and 6-8 have been cancelled and claims 1, 4, 10-15, 19, 23, 25-27, 30-32 and 38-39 have been amended. Hence, claims 1, 3-5, and 9-39 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

Applicant has amended the specification to address an objection by the Examiner and to insert serial numbers of U.S. Applications referred to in the cross reference to related applications section. No new matter is presented.

In the Claims

Claims 13-15

Although the Examiner indicated on the Office Action Summary that claims 1-39 were rejected, the Office Action does not provide any explanation of the basis for rejecting claims 13-15. Applicant respectfully points out that MPEP 706.07 admonishes examiners to keep in mind that the "applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed" before issuing a final rejection. Therefore, Applicant respectfully requests the Examiner to withdraw the rejection of claims 13-15, or supply the basis for the rejections in a subsequent non-final office action to enable Applicant to fairly respond to the Examiner's rejections of claims 13-15.

Rejections Under 35 U.S.C. §112, second paragraph

The Examiner rejected claim 19 under 35 U.S.C. 112 second paragraph as being indefinite. Applicant has amended the claim to distinctly claim the subject matter which applicant regards as the invention.

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1-3, 7-12, 16, 20, 23-29, and 32-39 under 35 U.S.C. 102(b) as being anticipated by Lynch, U.S. Patent No. 5,930,820 (hereinafter, *Lynch*). Applicant respectfully traverses the Examiner's rejections.

Lynch is directed to a microprocessor with a data cache that includes both a conventional storage (i.e., random access, non-LIFO storage) for storing non-stack data, and a stack storage (i.e., LIFO storage) for storing stack data. *Lynch*'s load/store unit sends push and pop commands to the data cache to manipulate stack data. The load/store unit also sends "stack access" commands to the stack storage to access stack data. The stack access commands are non-push/pop commands that access stack data by specifying an offset from the top of stack. See col. 6, lines 6-13. Because the stack storage has a finite size, the stack data requested by some pop or stack access commands may not be present in the stack storage of the data cache. In this situation, the data cache will send a retry signal to the load/store unit, in response to which the load/store unit will request the data from the conventional storage as a typical memory operation. The stack accesses satisfied from the conventional storage are slower than those satisfied from the stack storage because, unlike an access to the stack storage, the load/store unit must calculate a memory address to access the conventional storage. See col. 6, lines 23-39; col. 10, line 66 to col. 11, line 15. Importantly, the difference in access times is not attributable to whether the command is a pop instruction or a load instruction. Rather, the difference in access times is attributable to the fact that there are two separate storages, a LIFO storage and a non-LIFO storage, and to whether the stack data is present in the LIFO storage or the non-LIFO storage. Also importantly, the conventional storage and the stack storage are not arranged as first and second portions of a LIFO memory.

With respect to claim 1, Applicant has amended claim 1 to recite the limitation recited in claim 2, namely that the plurality of storage elements are configured as a last-in-first-out (LIFO) memory. Applicant has also amended claim 1 to recite the limitation of claim 7, which distinguishes between a pop instruction and a load instruction requesting to read data from the LIFO memory, as specified on the input. The LIFO memory provides data

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in a different number of clock cycles depending upon whether a pop or a load instruction requested to read the data, as recited in amended claim 1. Applicant respectfully asserts that *Lynch* does not teach a LIFO memory providing data in a different number of clock cycles depending upon whether a pop or a load instruction requested to read the data. Rather, *Lynch* teaches a LIFO memory that provides data in a first number of clock cycles and a non-LIFO memory that provides data in a second number of clock cycles, but not a LIFO memory that provides data in a different number of clock cycles depending upon whether a pop or a load instruction requested to read the data.

For these reasons, Applicant respectfully submits that amended claim 1 is not anticipated by *Lynch* and requests that the Examiner withdraw his rejection of claim 1. Claims 3-5 and 9 depend from claim 1 and recite further limitations, and therefore Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

With respect to claim 10, Applicant has amended the claim to clarify that if the source address of the requested source data hits in the first or second subset of the LIFO memory, the LIFO memory provides the requested source data in the first or second number of clock cycles, respectively. That is, in either case, the LIFO memory provides the data as long as the source data address hits in either the first or second subset of the LIFO memory.

To reject claim 10, the Examiner cited col. 3, lines 18-25 and col. 6, lines 23-29 of *Lynch*. Col. 3, lines 18-25 and col. 6, lines 23-29 of *Lynch* describe the data cache which is taught throughout *Lynch* which, as discussed above, includes two storages; the first is a conventional, non-LIFO storage for storing non-stack data, and the second is a LIFO storage for storing stack data. As discussed above, if the stack data requested by a pop or stack access command is not present in the stack storage, then the load/store unit will request the data from the conventional storage. The stack accesses satisfied from the conventional storage are slower than those satisfied from the stack storage. Importantly, the two storages of *Lynch*, i.e., the LIFO storage and the conventional storage, do not comprise first and second subsets of a LIFO storage, as the Examiner asserts. Therefore, these two storages of *Lynch* cannot be first and second subsets of a LIFO memory from

which data is provided in first and second respective different numbers of clock cycles, as recited in amended claim 10.

Furthermore, with respect to claim 10, Applicant has amended the claim to clarify that the address specified on the input is a memory address of the requested source data. The input memory address is compared with memory addresses of the data stored in the LIFO memory of claim 10.

To reject claim 10, the Examiner cited Address 64 of Fig. 3 of *Lynch* as an input specifying an address of source data requested from the cache memory. When *Lynch*'s load/store unit requests data from the stack storage, the Address 64 of Fig. 3 specifies an offset from the top of the stack, not a memory address. See col. 9, lines 29-33, 52-55. In fact, *Lynch* specifically teaches that data may be accessed via an offset from the stack memory without generating a memory address. See Abstract; col. 2, lines 49-51; col. 10, lines 25-26. Therefore, Applicant respectfully asserts that *Lynch* does not teach comparing a memory address of data requested from a LIFO memory with memory addresses of data cached in the LIFO memory to determine whether the requested data memory address hits in the LIFO memory based on the comparing, as recited in amended claim 10.

For these reasons, Applicant respectfully submits that amended claim 10 is not anticipated by *Lynch* and requests that the Examiner withdraw his rejection of claim 10. Claims 11-25 depend from claim 10 and recite further limitations, and therefore Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

With respect to claim 20, the Examiner asserts that *Lynch* teaches the recited limitation wherein the first subset of storage elements comprises a top one of the plurality of storage elements, citing col. 9, lines 52-56 of *Lynch*, and stating that when a standard pop command is performed, the top one of the storage elements is accessed. Col. 9, lines 45-51 describe how the stack storage provides data in response to a pop operation, which selects the top storage location of the stack storage; and col. 9, lines 52-56 describe how the stack storage provides data in response to a stack access, which selects a storage location below the top by an amount represented by an offset provided by the load/store

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unit. However, neither the cited texts of *Lynch* nor any other portion of *Lynch* teaches that the pop operation and the stack access operation take a different number of clock cycles. Therefore, Applicant respectfully asserts that *Lynch* does not teach a variable latency cache memory having a LIFO memory with a top storage element for caching stack data more recently pushed than data cached in a non-top subset of storage elements, such that if an input source data address hits in the top storage element, the cache memory provides the source data in a first number of clock cycles, but if the address does not hit in the top storage element then the cache memory provides the source data in a second number of clock cycles different from the first number of clock cycles, as recited in claim 20.

With respect to claim 26, Applicant has amended the claim to clarify that the virtual and physical addresses are memory addresses.

To reject claim 26, the Examiner cited col. 6, lines 23-39 of *Lynch*. As discussed above this portion of *Lynch*, as well as the remainder of *Lynch*, teaches that his data cache provides data with different access times because there are two separate storages, a LIFO stack storage and a conventional non-LIFO storage, and based on whether the stack data is present in the LIFO stack storage or the conventional non-LIFO storage since the load/store unit must calculate an address to access the conventional non-LIFO storage. Importantly, the cited portion of *Lynch* does not teach that his data cache provides data in first and second different clock cycles based on whether a virtual memory address and physical memory address hit in a LIFO memory, as recited in claim 26, and Applicant can find no such teaching in *Lynch*.

For these reasons, Applicant respectfully submits that amended claim 26 is not anticipated by *Lynch* and requests that the Examiner withdraw his rejection of claim 26. Claims 27-31 depend from claim 26 and recite further limitations, and therefore Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

With respect to claim 32, Applicant has amended the claim to recite the limitation that the cache memory is a last-in-first-out (LIFO) memory. Therefore, for reasons similar to those stated above with respect to claim 1, Applicant respectfully asserts that claim 32 is

not anticipated by *Lynch*. In particular, *Lynch* does not teach providing data from a LIFO memory in a different number of clock cycles depending upon whether a pop or a load instruction requested to read the data, as recited by amended claim 32. Rather, *Lynch* teaches a LIFO memory that provides data in a first number of clocks and a non-LIFO memory that provides data in a second number of clock cycles, but not a LIFO memory that provides data in a different number of clock cycles depending upon whether a pop or a load instruction requested to read the data.

For these reasons, Applicant respectfully submits that amended claim 32 is not anticipated by *Lynch* and requests that the Examiner withdraw his rejection of claim 32. Claims 33-37 depend from claim 32 and recite further limitations, and therefore Applicant respectfully requests that the Examiner withdraw his rejection of these claims.

Claim 38, as amended, recites a computer program product embodied on a computer-readable medium having computer readable program code for providing a variable latency cache memory as recited in amended claim 1. Therefore, for the reasons discussed above with respect to claim 1, Applicant respectfully asserts that claim 38 is not anticipated by *Lynch*.

Claim 39, as amended, recites a computer program product embodied on a computer-readable medium having computer readable program code for providing a variable latency cache memory as recited in amended claim 10. Therefore, for the reasons discussed above with respect to claim 10, Applicant respectfully asserts that claim 39 is not anticipated by *Lynch*.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of Healey, U.S. Patent No. 3,810,117 (herein after *Healey*). The Examiner rejected claim 22 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of Tremblay et al., U.S. Patent No. 6,038,643 (herein after *Tremblay*). The Examiner rejected claims 4-6, 17-19, and 30-31 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of Sager et al., U.S. Patent No. 6,425,055 (herein after *Sager*). Applicant respectfully traverses the Examiner's rejections.

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Claims 4-6 depend from independent claim 1, claims 17-19 and 21-22 depend from independent claim 10, and claims 30-31 depend from independent claim 26, respectively, which are not anticipated by *Lynch* as discussed above, and recite further limitations. Applicant, therefore, respectfully requests the Examiner withdraw his rejection of these claims.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1, 3-5, and 9-39 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,

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6/13/2006

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